Vivekananda College of Engineering & Technology
[Sponsered by Vivekananda Vidyavardhaka Sangha, Puttur (R)]
Affiliated to Visvesvaraya Technological University
Approved by AICTE New Delhi & Govt of Karnataka

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Preparatory Question Paper (CBCS Scheme)

USN: | 4 | V | P | 2 | 0 | C | S | 0 | 3 | 4 | SUB CODE: 18C

Third Semester B.E. Degree Examination, March. 2022

Computer Organization

TIME: 03 Hours Max. Marks:

Note: Answer any FIVE full questions, choosing ONE full question from each module.

MODULE 1

1 a. Write the basic performance equation. Explain the role of each parameters in the equation of the performance of the computer. **04 Marks**

b. Describe the basic operational concepts between processor and memory. **08 Marks**

c. Write a program to evaluate the arithmetic statement Y= (A+B) * (C+D) using three address, two address, one – address instructions. **08 Marks**

OR

2 a. What is an addressing mode? Explain any four addressing modes with examples. **08 Marks**

b. What is the effective address of the source operand in each of the following instructions,when the register R1 and R2 of computer contain the decimal value 1200 and 4600? **08 Marks**

(i) Load 20(R1), R5 (ii) Move #3000, R5 (iii) Store R5, 30(R1,R2)

(iv) Add –(R2), R5 (v) Subtract (R1)+, R5 .

c. With a memory layout starting at address "i" represent how "ABCD" data is stored inbig endian and little endian assignment scheme in a system of word length 16 bits. **04 Marks**

MODULE 2

3 a.What is bus arbitration? Explain distributed arbitration with a neat diagram. **08 Marks**

b. With supporting diagram; explain the following with respect to interrupts

i)Interrupt Nesting ii) Simultaneous requests. **08 Marks**

c. With a neat diagram, explain how to interface keyboard to the processor. **04 Marks**

OR

4 a.Explain the following the with respect to USB.

(i) USB Architecture (ii) USB Addressing **08 Marks**

b.With a neat diagram, explain about how data is read in asynchronous bus scheme. **07 Marks**

c.Write a short note on SCSI. **05 Marks**

MODULE 3

5 a. Explain direct mapped cache in mapping functions. 08 Marks

b. Draw and explain the internal organization of 2M*8 asynchronous DRAM chip. 08 Marks

c. What is memory interleaving. 04 Marks

OR

6 a. Define the following. 08 Marks
(i) Memory Latency (ii) Memory bandwidth (iii) Hit rate (iv) Miss penalty

b. Write a note on memory hierarchy with respect to speed, size and cost. 08 Marks

c. Calculate the average access time experienced by a processor if a cache hit rate is 0.88, miss penalty is 0.015 milliseconds and cache access time is 10 microseconds. 04 Marks

MODULE 4

7 Perform addition and subtraction of signed numbers.

a. i) (+4) and (-6) ii) (-5) and (-2) 08 Marks
iii)(+2) and (-3) iv)(+6) and (+3)

b. Explain the logic diagram of 4 bit carry look ahead adder and its operations 06 Marks

c. Perform bit pair recoding for (+14) and (-4) 06 Marks

OR

8 a.Perform Booth's Algorithm for signed numbers (-14) and (+11) 10 Marks

b. Write down the steps of restoring division algorithm. Apply restoring division algorithm on 25/4. 10 Marks

MODULE 5

9 a.Illustrate the sequence of operations required to execute the following instructions.
Add (R3), R1 10 Marks
b.Explain the three-bus organization of a data path with a neat diagram. 10 Marks

OR

10 a.Explain Hard Wired Control unit organization in a processing unit. 10 Marks

b.What is pipeline? Explain the four stages pipeline with its instruction execution steps and hardware organization. 10Marks